ABSTRACT OF THE DISCLOSURE

A circuit that may be used to implement boundary scan testing. The circuit generally comprises a pad circuit, a core logic, a cell, and a test circuit. The pad circuit may be configured to transfer a data signal in response to a pad control signal. The core logic may be configured to (i) exchange the data signal with the pad circuit and (ii) present a control signal. The cell may be configured to (i) transfer the data signal between the pad circuit and the core logic and (ii) swap the data signal and a test signal. The test circuit may be configured to (i) exchange the test data signal with the cell, (ii) store a test control signal, and (iii) multiplex the test control signal and the control signal to present the pad control signal.